Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Previously Presented) A microprocessor comprising:

a memory array having a stack for saving contextual data;

a central processing unit coupled to the memory array, the central processing unit having registers containing contextual data and a stack pointer and being arranged for saving contextual data upon a switch from a first to a second program in a variable number of registers that varies according to the value of at least one flag stored in a register to be saved.

2. (Original) The microprocessor according to claim 1 wherein the central processing unit is arranged for changing the value of the flag according to the content of a register, before saving contextual data contained in a variable number of registers that varies according to the value of the flag.

3. (Original) The microprocessor according to claim 2 wherein the central processing unit is arranged for changing the value of the flag according to the content of an extended addressing register of a program counter of the central processing unit.

4. (Original) The microprocessor according to claim 3 wherein the central processing unit is arranged for:

when the content of the extended addressing register is equal to 0, saving all the registers of the central processing unit containing contextual data, except for the extended addressing register; and

when the content of the extended addressing register is not equal to 0, saving all the registers of the central processing unit containing contextual data, including the extended addressing register.

5. (Original) The microprocessor according to claim 1 wherein the central processing unit is arranged for performing a test on the value of the flag so as to determine the number of registers to be saved.

6. (Currently Amended) The microprocessor according to claim 1 wherein the central processing unit is arranged for, upon the return to the first program:

restoring the register containing the flag at a first time; and

restoring contextual data contained in a variable number of registers that varies according to the value of the flag present in the restored register at a second time subsequent to the first time.

7. (Original) The microprocessor according to claim 1 wherein the central processing unit is arranged for saving the register containing the flag last.

8. (Original) The microprocessor according to claim 1 wherein the flag comprises at least one bit of a register containing condition code flags.

9. (Original) A method for managing the stack of a microprocessor having a central processing unit and a memory array, the central processing unit having registers containing contextual data and a stack pointer, the stack being a zone of the memory array dedicated to saving contextual data upon a switch from a first to a second program, the method comprising:

saving contextual data contained in a variable number of registers that varies according to the value of at least one flag stored in a register to be saved.

10. (Original) The method according to claim 9, comprising a step of:

changing the value of the flag according to the content of a register, before saving contextual data contained in a variable number of registers that varies according to the value of the flag.

11. (Original) The method according to claim 10 wherein the value of the flag is changed according to the content of an extended addressing register of a program counter of the central processing unit.

12. (Original) The method according to claim 11, comprising the following steps:

when the content of the extended addressing register is equal to 0, saving all the registers of the central processing unit containing contextual data, except for the extended addressing register; or

when the content of the extended addressing register is not equal to 0, saving all the registers of the central processing unit containing contextual data, including the extended addressing register.

13. (Original) The method according to claim 9, comprising a step of:

testing the value of the flag for determining the number of registers containing the data to be saved.

14. (Original) The method according to claim 9, comprising the following steps:

restoring the register containing the flag; then

restoring contextual data contained in a variable number of registers that varies according to the value of the flag present in the restored register.

15. (Original) The method according to one claim 9 wherein the register containing the flag is saved last and is restored first.

16. (Original) The method according to claim 9 wherein the flag is formed by at least one bit of a register containing condition code flags.

17. (Previously Presented) A microprocessor comprising:

a memory array having stored therein contextual data;

a central processing unit coupled to the memory array;

a plurality of registers associated with the central processing unit, a first group of the registers storing contextual data and a second group of the registers not storing contextual data when a flag has a first value and switching to store contextual data also in the second group of registers when the flag switches to a second value, such that the number of registers that store contextual data is variable

and where the flag is stored in a register to be saved as part of the program contextual data;

a stack pointer associated with the central processing unit and being arranged for directing contextual data to be stored in the first group only or in both the second group and the first group, based on the flag value.

18. (Original) The microprocessor according to claim 17 wherein the second group of registers includes a register which is used as an extended addressing register when the flag is at a first value.

19. (Original) The microprocessor according to claim 17 wherein the second group of registers includes a single register.

20. (New) A microprocessor comprising:

a memory array;

a central processing unit coupled to the memory array;

a first group of registers associated with the central processing unit and arranged to store contextual data;

a second group of registers associated with the central processing unit and arranged to store contextual or non-contextual data; and

a flag defined in the first group of registers;

wherein the central processing unit is arranged to suspend execution of a first program and commence execution of a second program and the central processing unit is further arranged to store the first group of registers in the memory array and conditionally store a variable number of registers of the second group of registers in the memory array.

21. (New) The microprocessor according to claim 20 wherein the flag is used to determine if the second group of registers are arranged to store contextual data.

22. (New) The microprocessor according to claim 21 wherein the second group of registers is only stored in the memory array if the flag has a first value.

23. (New) The microprocessor according to claim 20 wherein the flag is used to indicated if the second group of registers are arranged to store contextual data.

24. (New) The microprocessor according to claim 23 wherein the flag is loaded with a first value only if the second group of registers are arranged to store contextual data.